BSIM3v3.2 Model

Enhancements and Improvements Relative to BSIM3v3.1

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This document describes in detail the enhancements and improvements of BSIM3v3.2 relative to BSIM3v3.1, including a table of new model parameters, model enhancements, code implementations, bug fixes and a summary on backward compatibility with BSIM3v3.0 and BSIM3v3.1.

I. New Model Parameters in BSIM3v3.2

Table 1 New model parameters in BSIM3v3.2

Symbol in equation	Symbol in Spice	Description	Default value	Binning option
toxm	toxm	Gate oxide thickness tox value at which parameters are extracted	tox [m]	No
vfb	vfb	DC flat-band voltage	Calculated [V]	Yes
noff	noff	CV parameter in *VgsteffCV* for week to strong inversion region	1.0	Yes
voffcv	voffcv	CV parameter in *VgsteffCV* for week to strong inversion region	0.0	Yes
ijth	ijth	Diode limiting current	Calculated [A]	No
$\alpha 1$	Alpha1	Substrate current parameter	0.0 [V^{-1}]	Yes
acde	acde	Exponential coefficient for charge thickness in the accumulation and depletion regions	1.0 [m/V]	Yes
moin	moin	Coefficient for the gate-bias dependent surface potential	15.0 [$V^{1/2}$]	Yes
tpb	tpb	Temperature coefficient of pb	0.0 [V/K]	No
tpbsw	tpbsw	Temperature coefficient of pbsw	0.0 [V/K]	No
tpbswg	tpbswg	Temperature coefficient of pbswg	0.0 [V/K]	No
tcj	tcj	Temperature coefficient of cj	0.0 [1/K]	No
tcjsw	tcjsw	Temperature coefficient of cjsw	0.0 [1/K]	No
tcjswg	tcjswg	Temperature coefficient of cjswg	0.0 [1/K]	No

Table 1 New model parameters in BSIM3v3.2 (Continued)

Symbol in equation	Symbol in Spice	Description	Default value	Binning option
Llc	Llc	Coefficient of length dependence for CV channel length offset	DC Ll [m^{Lln}]	No
Lwc	Lwc	Coefficient of width dependence for CV channel length offset	DC Lw [m^{Lwn}]	No
Lwlc	Lwlc	Coefficient of length and width cross-term for CV channel length offset	DC Lwl [$m^{Lwn+Lln}$]	No
Wlc	Wlc	Coefficient of length dependence for CV channel width offset	DC Wl [m^{Wln}]	No
Wwc	Wwc	Coefficient of width dependence for CV channel width offset	DC Ww [m^{Wwn}]	No
Wwlc	Wwlc	Coefficient of length and width cross-term for CV channel width offset	DC Wwl [$m^{Wln+Wwn}$]	No

II. Enhancements of BSIM3v3.2 Relative to BSIM3v3.1

(1) A new intrinsic capacitance model (the Charge Thickness Model) considering the finite charge layer thickness determined by quantum effect is introduced as capMod 3. It is very accurate in all operating regions.

This model is smooth, continuous and accurate throughout all regions. The model parameter capMod defaults to 3. CapMod 0, 1 and 2 are retained to maintain backward compatibility with BSIM3v3.1.

(2) Improved modeling of C-V characteristics at the weak-to-inversion transition.

Two transition parameters "n_{off}" and "v_{offcv}" are introduced into $V_{gsteffCV}$ to adjust the CV curve shape around $V_{gs} \approx V_{th}$ as

$$V_{gsteffCV} = n_{off} \cdot n \cdot Vtm \cdot \log\left(1 + \exp\left(\frac{V_{gse} - V_{th} - v_{offcv}}{n_{off} \cdot n \cdot Vtm}\right)\right)$$

where n_{off} defaults to 1.0 and v_{offcv} defaults to 0.0 for backward compatibility; if ($n_{off} < 0.1$) and ($n_{off} > 4.0$), or if ($v_{offcv} < -0.5$) and ($v_{offcv} > 0.5$), warning messages will be given. $V_{gsteffCV}$ has been re-implemented to avoid any potential discontinuities and numerical instabilities.

(3) Adding the t_{ox} dependence into the threshold voltage V_{th} model.

t_{ox} dependence is introduced in the model parameters K_1 and K_2. V_{th} therefore becomes

$$V_{th} = V_{th0ox} + K_{1ox} \cdot \sqrt{\Phi_s - V_{bseff}} - K_{2ox} \cdot V_{bseff}$$
$$+ K_{1ox} \cdot \left(\sqrt{1 + \frac{Nlx}{L_{eff}}} - 1 \right) \cdot \sqrt{\Phi_s} + \Delta V_{th}$$

with

$$V_{th0ox} = V_{th0} - K_1 \cdot \sqrt{\Phi_s}$$
$$K_{1ox} = K_1 \cdot \frac{t_{ox}}{t_{oxm}}$$
$$K_{2ox} = K_2 \cdot \frac{t_{ox}}{t_{oxm}}$$

where t_{oxm} has a default value of t_{ox}; if t_{oxm} is equal to or smaller than zero, a fatal error message will be given; ΔV_{th} term represents V_{th} variation due to the short/narrow channel effects and DIBL.
The above equations improve the scalability of V_{th} model with respect to t_{ox}.

(4) Adding flat-band voltage (v_{fb}) as a new model parameter to accurately model MOSFETs with different gate materials.

v_{fb} defaults to the following for backward compatibility:
if (V_{th0} is given), then vfb will be computed from V_{th0};
Else v_{fb} = -1.0.

(5) Improved substrate current scalability with the channel length. I_{sub} is now expressed as

$$I_{sub} = \frac{\alpha_0 + \alpha_1 \cdot L_{eff}}{L_{eff}} \cdot \left(V_{ds} - V_{dseff}\right) \cdot \exp\left(\frac{-\beta_0}{V_{ds} - V_{dseff}} \right) \cdot I_{dsa}$$

where the new parameter α_1 defaults to 0.0 for backward compatibility with BSIM3v3.1 and I_{dsa} is the source-drain current without the substrate current induced body bias effect.

(6) Restructuring the non-quasi-static (NQS) model, addition of NQS in the pole-zero

analysis and fixing NQS bugs.

The NQS model is re-implemented. A new charge partitioning scheme is used which is physically consistent with that in the quasi-static C-V model and significantly improves the simulation performance. The parameter nqsMod is now an element (instance) parameter, no longer a model parameter.

(7) Adding the temperature dependence in the diode junction capacitance model, where both the unit area junction capacitance and built-in potential are now temperature dependent as:

```
deltT = ckt->CKTtemp - model->BSIM3tnom;
Cj(T) = Cj(tnom) * (1 + tcj * deltT)
Pb(T) = Pb(tnom) - tpb * deltT
Cjsw(T) = Cjsw(tnom) * (1 + tcjsw * deltT)

Pbsw(T) = Pbsw(tnom) - tpbsw * deltT
Cjswg(T) = Cjswg(tnom) * (1 + tcjswg * deltT)
Pbswg(T) = Pbswg(tnom) - tpbswg * deltT
```

The above equations are evaluated in b3temp.c file.
Default model (all new parameters set to zero) is identical to BSIM3v3.1.

(8) The DC junction diode model now supports a resistance-free diode model and a current-limiting feature.

A current limiting parameter *ijth* is introduced which corresponds to two critical voltages: *vjsm* and *vjdm*. BSIM3 will calculate *vjsm* and *vjdm* depending on the value of *ijth*. For the S/B diode,

If *ijth* is specified to be zero, a resistance-free diode model will be triggered;

Else if *ijth* is given and larger than zero,

$$Vjsm = Nvtm \cdot log\left(1 + \frac{Ijth}{I_s}\right)$$

Else *ijth* not specified, *vjsm* = 0.5V (**backward compatible with BSIM3v3.1**), and *ijth* is computed by

$$ijth = I_s \cdot \left(exp\left(\frac{0.5}{Nvtm}\right) - 1\right)$$

S/B diode current can therefore be expressed by

$$I_{diode} = I_s \cdot \left(exp\left(\frac{V_{bs}}{Nvtm}\right) - 1\right) + G_{min} \cdot V_{bs} \qquad (V_{bs} < vjsm)$$

$$I_{diode} = Ijth + \frac{Ijth + Is}{Nvtm} \cdot (Vbs - Vjsm) + G_{min} \cdot V_{bs} \qquad (V_{bs} > vjsm)$$

The same holds for the D/B diode.
If *ijth* < 0.0, a fatal error message will be given.

(9) Option of using C-V inversion charge equations of capMod 0, 1, 2 or 3 to calculate the BSIM3 thermal noise when noiMod == 2 or 4. The old channel charge equation is removed; backward compatibility is not kept by advice from the Compact Model Council.

(10) Elimination of the small negative capacitance of C_{gs} and C_{gd} in the accumulation-depletion regions.

A zero-bias *vfbzb* calculated from V_{th} is used in capMod 1, 2 and 3 when BSIM3version == 3.2. If BSIM3version < 3.2, the old bias-dependent *vfb* is kept for capMod 1 and 2 for backward compatibility; capMod 3 does not support the old bias-dependent *vfb*.

(11) Introducing a separate set of length/width dependence parameters (*Llc*, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc*) for CV channel length and width to better fit the capacitance data.

Llc, *Lwc*, *Lwlc*, *Wlc*, *Wwc* and *Wwlc* default to the corresponding DC parameters *Ll*, *Lw*, *Lwl*, *Wl*, *Ww* and *Wwl*, respectively, for backward compatibility.

(12) Adding parameter checking to avoid bad values for certain parameters as:

If *psccbe*2 <= 0.0, the user will be warned of the poor value used.
If (*moin* < 5.0) or (*moin* > 25.0), a warning message will be given.
If (*acde* < 0.4) or (*acde* > 1.6), a warning message will be generated.
If (*noff* < 0.1) or (*noff* > 4.0), a warning message will be given.
If (*voffcv* < -0.5) or (*voff cv* > 0.5), a warning message will be given.
If (*ijth* < 0.0), fatal error occurs.
If (*toxm* <= 0.0), fatal error occurs.

The recommended parameter ranges for *acde*, *moin*, *noff* and *voffcv* can be found from above.

(13) Bug fixes.

Table 2 lists the bug fixes in BSIM3v3.2 relative to BSIM3v3.1.
Since the NQS model has been re-implemented, bug fixes for NQS part are not provided.

Table 2 Bug fixes in BSIM3v3.2

Bug Description	Involved C files in BSIM3v3.1	Bug Reporter	Bug Fixing by	Bug Fixing Date
Pd and *Ps* clamps result in non-convergence for some special circuits	b3check.c	Junichi Ohtani (Sony)	Junichi Ohtani (Sony)	March 1997
BSIM3gbd should be removed from *(here->BSIM3SPdpPtr)	b3ld.c	Weidong Liu (UCB)	Weidong Liu (UCB)	March 1997
"w" is missing in ldvt0w	b3mpar.c	Shin-Long Shen (TSMC)	Shin-Long Shen (TSMC)	June 1997
Leff should be *LeffCV* for abulkCVfactor	b3temp.c	Min-Chie Jeng (Cadence)	Min-Chie Jeng (Cadence)	November 1997
"Vbm is ignored because K1 or K2 is given" should be removed, since vbm is still used to limit Vbseff in b3temp.c file.				October 1997
"ckt->CKTgmin" should be removed from "ceqbs" and "ceqbd"	b3ld.c	Min-Chie Jeng (Cadence) Peter Lee (Hitachi)	Min-Chie Jeng (Cadence) Peter Lee (Hitachi)	November 1997
"vgs = pParam->BSIM3vth0 + 0.1" should be "vgs = model->BSIM3model * pParam->BSIM3vth0 + 0.1" in b3ld.c file, reported and fixed by Peter Lee of Hitachi, May 1998.				
Isub swapping	b3ld.c	Min-Chie Jeng (Cadence)	Min-Chie Jeng (Cadence)	May 1998
Isub was ignored in AC and Pole-Zero analysis	b3acld.c & b3pzld.c	Weidong Liu (UCB)	Weidong Liu (UCB)	May 1998

III. Summary on Backward Compatibility

(1) Backward compatibility with BSIM3v3.1

Even when all new model parameters are given their default values, the following code modifications could result in inconsistencies between BSIM3v3.2 and BSIM3v3.1:

re-implementation of NQS model (Item 6);
using CV *Qinv* for BSIM3 thermal noise evaluation (Item 9);
zero-bias *vfbzb* for capMod 1 and 2 (through BSIM3version number control) (Item 10);
Removing of *Pd* and *Ps* clamps (Item 13);
using *LeffCV* for abulkCVfactor (Item 13);

removing here->BSIM3gbd from "*(here->BSIM3SPdpPtr)" (Item 13);
removing ckt->CKTgmin from "ceqbs" and "ceqbd" (Item 13);
fixing of "vgs = pParam->BSIM3vth0 + 0.1" term in b3ld.c file (Item 13); and
Isub bug fixing in b3ld.c, b3acld.c and b3pzld.c (Item 13).

(2) Backward compatibility with BSIM3v3.0

Current users of BSIM3v3.0 may migrate to BSIM3v3.2 directly by passing BSIM3v3.1. The compatibility of BSIM3v3.2 to BSIM3v3.0 is summarized by the above list (**Backward compatibility with BSIM3v3.1**) plus the summarized information on compatibility between BSIM3v3.1 and BSIM3v3.0 (*Differences between BSIM3v3.1 and BSIM3v3.0*, which can be found in **BSIM3 version 3.1** section by clicking on "**Archive: FTP**" on this site).

BSIM3 web site: ***http://www-device.eecs.berkeley.edu/~bsim3***

Compact Model Council web site: ***http://www.eia.org/eig/CMC***

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